Bryce Tobiano

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SKILLS: C++, Java, React. js, Express. js, JavaScript, HTML, CSS, Python, MATLAB, Git, Verilog, VerilogHDL

EDUCATION

University of Southern California, Viterbi School of Engineering

BS in Computer Engineering and Computer Science GPA: 3.86/4.00

- Organizations: HackSC, Christian Students at USC, Society of Asian Engineers and Scientists, •
- Relevant Coursework: Algorithms, Data Structures, Distributed Systems for IoT, SoC, MOS VLSI •

EXPERIENCE

Hibiscus - HackSC

- Software Engineer Led team of four developers to develop Hibiscus, an all-in-one, plug-and-play hackathon platform, used by 800+ users using Next.JS, React, Node.JS, Express.js, and Supabase.
- Deployed a Supabase backend which tracks user status, event participation, and other statistics.
- Redesigned and refactored NextJS frontend pages for events, sponsors, and judging utilizing.

Evidant Corporation

Software Engineer and Data Science Intern

- Collaborated with a team of 6 engineers to implement Angular components and revamped C# backend to create a dashboard allowing analysts to manipulate data using custom functions through a **data transformer**.
- Established **data frame** and **pivot table** processing within Angular components by building upon Python pandas library for improved speed and parsing capabilities.
- Improved data processing by a factor of 25% from ~2secs to ~1.5secs per 10,000 lines through optimized function calls and implementing multiprocessing capabilities.

John O'Connor Nanofabrication Laboratory

Cleanroom Fabrication Intern

- Optimized fabrication process of memristors through testing a variety developing and lift off chemicals resulting in 25% more yield and a 50% increase in durability.
- Handled cleanroom tools such as RIE80 Oxford Etcher, Lithographers, EBeam Evaporators, Sputtering,

USC Viterbi School of Engineering

EE250 Course Producer (Distributed Systems and the Internet of Things)

Revamped weekly labs and held weekly office hours on various Systems and IoT topics and protocols using tools including TiG IoT monitoring, MQTT, Cloud Computing AI, TCP, UDP, and PCB Design.

PROJECTS

Convolutional Neural Network on an FPGA - EE454 System-on-Chip

- Synthesized a Verilog implementation of a Convolutional Neural Network onto a Altera DE2-115 FPGA to identify features handwritten digits (MNIST dataset), achieving 85% accuracy.
- Optimized computational resources to fit CNN architecture within FPGA constraints, achieving efficient data flow and resource management.

Systolic Array Chip Design - EE477 MOS VLSI

- Constructed transistor-level layout of a systolic array via Cadence Virtuoso for compute-heavy tasks such as deep learning and matrix multiplication.
- Improved power consumption by 35%, area by 25%, and performance by 35% using iterative design strategies.

Firing Frenzy - EE354 Digital Circuits

- Implemented a target practice game in Verilog for Digilent Nexys 4 FPGA.
- Retrieved 3-axis accelerometer data via SPI protocol and interfaced with VGA output.
- Designed a comprehensive **state machine** to account for all game states, display, and other connections.

Laguna Hills, CA *May* 2023–July 2023

Los Angeles, CA

Los Angeles, CA

May 2024–August 2024

July 2024–Present

November 2024

November 2024

May 2024

Los Angeles, CA Expected May 2026

U.S. Citizen

September 2022–Present

Los Angeles, CA